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BIETECH VOICE

Department of ECE

A HALF YEARLY NEWSLETTER OF ELECTRONICS & COMMUNICATION ENGG.

Volume – 5, Issue – 1 July – December2021

Vision: To be in the forefront in providing quality technical education and research in Electronics & Communication Engineering to produce skilled professionals to cater to the challenges of the society.

Inside the Issue

Quote Corner

"The future depends on what we do in the present"

Chairman/ Editor
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Mission:

M1. To facilitate the students with profound technical knowledge through effective teaching learning process for a successful career.

M2. To impart quality education to strengthen students to meet the industry standards and face confidently the challenges in the program.

M3. To develop the essence of innovation and research among students and faculty by providing infrastructure and a conducive environment.

M4. To inculcate the student community with ethical values, communication skills, leadership qualities, entrepreneurial skills and lifelong learning to meet the societal needs.

Innovation and Design Thinking

Innovation is the process of generating new and unique ideas or solutions and applying them to create value for the service.

Design thinking is a term used to denote a set of strategic, conceptual, and practical processes in which design concepts are developed (product proposals, structures, equipment, communications, etc.).

Any individual who has the following traits can be design thinker in the organizations, namely

1. Individual who has the concern for the individuals and who know the working challenges in at workplace
2. Knowledge of multi -functionality of the organization
3. Vision for developing right process in the organization
4. Capability to understand the problems on the job and ability to work on the problems related to the jobs of the organization.

There are five stages to the design thinking process

Benefits of Design Thinking

1. It helps to overcome creative challenges: Design Thought gives the freedom to look at problems in many ways. It involves a lot of brains to come up with the best ideas, which helps to improve students' knowledge.
2. Helps to meet customer requirements effectively: design thinking involves developing prototypes when testing and using customer feedback repeatedly to ensure quality assurance. By following a successful design idea, the product will eventually meet the needs of customers.
3. It helps us to increase the knowledge of Design Thinking: will do a lot of experiments in the design thinking process. We will always try to improve the model by using customer feedback to ensure customer satisfaction.

From HOD's Desk

I am happy that we are bringing out the first issue of volume 5.I would like to congratulate our alumni Mr. Harsha Manjunath for being a resource person during FDP on Introduction to Microchip FPGA.

Under the Gnana Vrudhi lecture series, faculty delivered talk on Image processing domain.

Best research paper award was received for the paper entitled Design and verification of CMOS LDO regulator, carried out by final year students.

Also I would like to share that webinars were conducted for the VI sem students to create awareness and guide students to select their Internship domain.

Congratulate the VTU rank holders Darshan A Hadadi & Aishwarya K M for the year 2019 & 2020 respectively.

DEPARTMENTAL ACTIVITIES

Gnana Vrudhi- Lecture Series

- Ganesh K has delivered a lecture on C**hallenges in Video Quality Assessment** on 23rd August 2021.

- Webinar was organized for IV sem students on **Android Application Development** on 3rd August 2021. The resource person was Mr. Rishi kethu Chand IV sem student of the department. The event was coordinated by **Dr. G S Sunitha Prof & HOD.**
- Webinar on **Mentor Graphics VLSI Tool** was delivered by Bharath Kumar B Y, Sharan and Bhanu Prakash of Core EL Technologies. The event was coordinated by **Dr. G S Sunitha Prof & HOD** on 4th August 2021.
- **NBA online evaluation process** completed on 8th to 10th October 2021. Dr. **Vineeth Sahula, Professor in E&CE** from **Malaviya National Institute of Technology, Jaipur** was the expert for E&CE Department.
- Webinar **on Introduction to MEMS Sensors** was delivered by Dr. Nithin S Kale, Cofounder and Chief Technology Officer, Nano Swift Technologies Pvt. Ltd. The event was coordinated by **Dr. G S Sunitha Prof & HOD** on 29th October 2021.

EC Forum Inauguration, welcome to III & V semester students and felicitation to VTU rank holders Darshan A Hadadi & Aishwarya K M for the year 2019 & 2020 respectively. was organized under EC forum on 20th November 2021.

Inauguration of ECForum

Guest:
Mr. Waseem Akram B
Mrs. Ashwini P.A

Felicitation to VTU Rank Holders

- Mirza Quadir Baig, Alumnus 2016, Area officer, Krishnapatnam port, Indian Railway traffic service, Ministry of Railways, Govt. of India, presented an **Awareness Session on Competitive Exams** to V sem students on 02nd November 2021.

Awareness session on Competitive Exams by Mirza Quadir Baig, alumnus 2016

- Siddanagowda G N, Alumnus-2015, Manager, Western Digital, Bangalore, conducted training session for V sem students on **Embedded System** from 27th November 2021, every Saturday for a duration of four weeks.

Training session on Embedded System by Siddanagowda G N, Alumnus-2015

- Students of V and VII semester along with faculty visited the **BEL Bengaluru** on 17th December 2021, on the occasion of 75 years of independence.

Industrial Visit to BEL Bengaluru

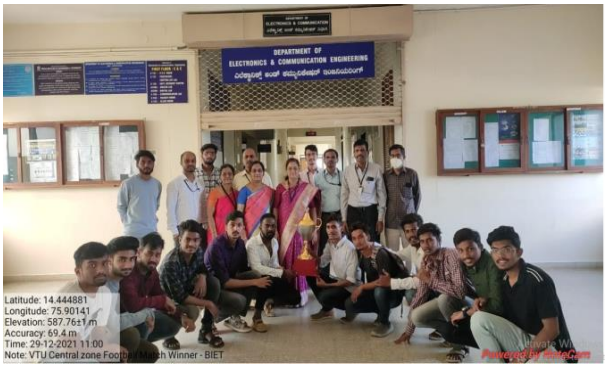
FDP/WORKSHOP ORGANIZED

- National Level One Week Online Faculty Development Program on **Introduction to Microchip FPGA** from 19th to 23rd July 2021 was organized by ECE Research Centre, Department of Electronics & Communication Engineering in association with ISTE, Faculty Chapter BIET, IETE Shivamogga Center & Tecnomic Components Pvt. Ltd., Bengaluru. The resource person was Mr. Harsha Manjunath, Senior Field Application Engineer, Tecnomic Components Pvt. Ltd.**,** Bengalore. Under the guidance of Dr. G S Sunitha, the program was coordinated by **Dr. Leela G H, Dr. Nirmala S O and Savithri G R.**
- Two Days Workshop in blended mode on **Implementation of NEP 2020** on 10th & 11th Dec 2021 was organized by BIET in association with VTU, Belgavi. The program was coordinated by Dr. G P Desai, **Dr. G S Sunitha** and Dr. Vinutha H P

FDP on Introduction to Microchip FPGA

STUDENT ACHIEVEMENTS AND ACTIVITIES

- Students of VI sem attended BootCamp organized by BIET in association with Startup Karnataka and NAIN on 5th June 2021.
- Ashwini V Jayashetty and Chinmayraj of V sem have qualified **NPTEL online certification** for the course on **Introduction to Internet of Things** during July – October 2021.
- Bhoomika H and Manoj Nagaraj Kasal of V sem have qualified **NPTEL online certification** for the course on **Digital Circuits** during July – October 2021.
- Chandan, Suhas and Om Praveen Panade were part of the football team from BIET and are winners in **VTU Center Zone Football Match against MCE Hassan** held on 28th December 2021.



VTU Center Zone Football Match Winners

PLACEMENT ACTIVITIES

- Campus Recruitment of 2020-21 batch Students.

Sl.No.	Name of the company	No. of students Placed
1	SLK	04
2	TCS DIGITAL	02
3	MAPLELABS	01
4	WIPRO	10
5	TCS NINJA	07
6	KPMG	10
7	ROBOSOFT	01
8	SILVER PEAK	04
9	HERIN ELECTRONICS	08
10	Altimetrix	02
11	Gigsky	01
12	Zensar	02
13	Quest Global	10
14	Capgemini	03
15	KnodTec	01
16	Sonata SOftware	06
17	FAI	01
18	Infosys(off Campus)	13
Total		86

Co-Curricular Activities

- Final year project batch students Shreevatsa N S, Veeresh Banakar and Shravya N presented a paper **Design and verification of CMOS LDO regulator at** 2nd International Virtual Conference on Emerging Trends in Science, Engineering and Management-2021 on 15th and 16th July 2021 and received the **Best Research Paper Award.**
- Final year project batch students Shreesha N S, Adithya Bangur, Swathi K S and Srujana Kandagal presented a paper on **Design and Implementation of BiCMOS based band gap reference circuit** at 2nd International **Virtual** Conference on Emerging Trends in Science, Engineering and Management-2021 on 15th and 16th July 2021.
- Final year students Madhu NP, Mamatha Sarathi P, T Srinivas Koushik, Praveen KR have participated in **National Project Exhibition SKIT EXPO - 2021**, organized by R & D Cell of SKIT Bangalore on 04th August 2021.
- 9 Project batch students participated in **NIRMANA 1.0** project exhibition held on 13th August 2021. Sri Nagaraja G K, Alumnus of the institute from batch 1994 presently working as Techno Programmer, Tata Communications Ltd, Banglore was the Expert member. The project entitled **IoT Based Real time System to Monitor Quality of Milk** carried out by Karthik Dhulashetty, Praveen N, Prerana R S and Pooja A R, under the guidance of Dr. G S Sunitha Prof. & Head was selected as **Best Project.**
- Eight projects have been exhibited in Open house project Exhibition **Technovation-21** on 04th September 2021.

Technovation-21

FACULTY ACHIEVEMENTS AND ACTIVITIES

- Ganesh K was the resource person for invited talk on **Internet of Things - Futuristic Perspective** organized by Dept of E&CE, Brindavan College of Engineering, Bengaluru on 25th November 2021.

Research Activities

- Prof. Banumathi K L completed Ph.D. **Open Seminar-1**on 19th July 2021.
- Prof. Kiran Kumar G H completed Ph.D. **Pre-submission Colloquium** on 11th August 2021.
- Under the guidance of Dr. G S Sunitha Prof. & HOD, Prof. Prakash K M has completed **Ph.D. Pre-submission Colloquium** on 04th December 2021.
- Prof. Banumathi K L and Prof. Ganesh K submitted **Ph.D. Thesis** on 22nd December 2021.
- Prof. Kiran Kumar G H has submitted **Ph.D. Thesis** on 28th December 2021.
- Under the guidance of Dr. G S Sunitha Prof. & HOD, Prof. Prakash K M has submitted **Ph.D. Thesis** on 31st December 2021.

Workshops/FDP Attended

- Mr. Kantharaj S P has attended a webinar on **Effective utilization of VTU Consortium E-Resources using RRCE** on 2nd July 2021.
- Mrs. Bhagya Shanthakumar has attended Xilinx webinar on **Pynq - Python productivity for Zynq SoC and Zynq Ultrascale+ MPSoC** in association with CoreEL Technologies and Xilinx on 09th July 2021.
- Mr. Ali I K has attended **Universal Human Values in Technical Education** organized by AICTE from 12thto 16thJuly 2021.
- Dr. Sunitha G S, Dr. Leela G H, Mr. Prakash K M and Mr. Lingraj have participated in Mentor Graphics webinar on **Full Custom and Semi-custom Design Flow** in association with CoreEL Technologies and Mentor Graphics organized by CoreEl Technologies on 15th July 2021.
- Dr. Leela G H, Dr. Nirmala S O, Mr. Prakash K M, Mr. Kiran Kumar G H, Mrs. Banumathi K L, Mrs. Radhika Priya Y R, Mr. Lingraj and Mr. Yogesh K O have attended AICTE Training and Learning (ATAL) Academy Online Elementary FDP on **VLSI -IP DESIGN Approach to SRAM Compiler Design** organized by GM Institute of Technology, from 16th to 20th August 2021.
- Mrs. Bhagya Shanthakumar has attended5 Day National Level Online Faculty Development Programme on **Current Research Trends in VLSI Design and Device Modelling** organized by Department E&CE, Atria Institute of Technology, Bangalore from 24th to 28thAugust 2021.
- Mr. Kantharaj S P has attended a webinar on **Artifact Innovation and Development using Additive Manufacturing and IoT** organized by Manipal University on 23rd August 2021.
- Mrs. Nirmala Gand Mrs. Suman B S have attended a FDP on **Digital VLSI Design and Verification** organized by Bangalore Institute of Technology, Bangalore from 23rd to 27thAugust 2021.
- Mrs. Vanishree H V has attended a FDP on **Recent Trends in Control System Engineering** organized by Chatrapathi Shivaji Institute of Technology, Chhattisgarh from 23rd to 27th August 2021.
- Dr. Sunitha G S and Dr. Jayadevappa B M have attended a **Student Empowerment Program** CSR Initiative organized by Honeywell and ICT on6thSeptember 2021.
- Mrs. Poornima G N has participated in AICTE Training and Learning (ATAL) Academy Online Elementary FDP on **Internet of Things in 5G Wireless Communication** from 06th to 10th September 2021, organized by North Eastern Regional Institute of Science and Technology (NERIST) Nirjuli, Arunachal Pradesh.

- Mrs. Banumathi K L has participated in five days Faculty Development Program on **Developing Leadership Skills for Enhancing Personal and Organizational Outcome** conducted by Department of E&CE, VVCE, Mysore from 13th to 17thSeptember 2021.
- All faculty members of E&CE department attended a Webinar on **Introduction to MEMS Sensors**, organized by department of E&CE BIET, Davangere on 29thOctober 2021.
- Mrs. Sucharitha S D has attended a FDP on **Recent Trends in Machine Learning and Pattern Recognition** organized by GMIT, Davangere from 6th to 11th December 2021.
- All faculty members of E&CE department attended Two Day Workshop on **Implementation of National Education Policy-2020**, organized by BIET Davangere on 10th and 11th December 2021.
- Dr. G S Sunitha, Dr. Nirmala S O, Mr. Prakash K M, Mrs. Suma K G, Mrs. Radhika Priya Y R, Mrs. Banumathi K L and Mrs. Bhagya Shanthakumar have attended **An Overview of Teaching Techniques in Basic Electronics and Communication Engineering** organized by AICTE-VTU, Muddenahalli, from 13th to 17th December 2021.
- Mrs. Banumathi K L has attended a FDP on **Recent Trends in Machine Learning and Pattern Recognition** organized by GMIT, Davangere from 6th to 11th December 2021.
- Mr. Mahendrachari, Mr. Ranjith Patil N and Mrs. Vanishree H V have attended two days workshop on **Universal Human Values and Professional Ethics** organized by department of Civil Engineering BIET Davangere on 29th and 30th of November 2021.

ARTICLE

- Shreevatsa N S, Veeresh Banakar and Shravya N, Dr. G S Sunitha presented a paper **Design and verification of CMOS LDO regulator at** 2nd International Virtual Conference on Emerging Trends in Science, Engineering and Management-2021 on 15th and 16th July 2021 and received the **Best Research Paper Award.**

  Abstract: This paper presents a design of a low dropout regulator based on a 180 nm standard CMOS process. The LDO design has a dropout of 110 mV and produces a constant output of 1.5 V. The circuit makes use of a two-stage miller compensated error amplifier which is designed to have a gain of 60 dB and a phase margin of around 60º. PMOS pass element has been selected. The circuit exhibits a load regulation of 9.4527 mV/A (i.e., 0.031 %) with typical and maximum load currents being 25 mA and 50 mA respectively. The line regulation of the circuit is 912.7396µV/V for an input variation of 1.6V to 2 V. The designed circuit makes use of dominant pole compensation technique to make the whole system stable and has a maximum gain of 81 dB and phase margin of 72º while the circuit has a gain bandwidth of 117 kHz and has the worst-case power supply rejection ratio (PSRR) of [76 dB, 55.71 dB] @ [100 Hz, 251 kHz] in full load condition. The circuit dissipates a total power of 6.0081mW. The circuit grounds a quiescent current of 5 µA.

- Shreesha N S, Adithya Bangur, Swathi K S and Srujana Kandagal, Dr. Nirmala S O presented a paper on **Design and Implementation of BiCMOS based band gap reference circuit** at 2nd International **Virtual** Conference on Emerging Trends in Science, Engineering and Management-2021 on 15th and 16th July 2021.

  Abstract: All analog circuits use “golden reference”, which are extensively used for biasing. This paper presents a first-order Bandgap reference (BGR), realized in two different architectures – using Cascode Current Mirror and using two stage Op – Amp where the Op – Amp is miller compensated and produces a gain of 60 dB with phase margin of 60º. 180 nm

standard CMOS process is used to implement the circuit. The BGR produces a constant output reference voltage of 1.18 V when designed using Cascode Current Mirror architecture, while 1.10 V in Op – Amp based architecture. Cascode Current Mirror based BGR has a Temperature Coefficient of 21.83 ppm for a wide range of -20º to 100º and 50ppm for Op – Amp based BGR. The line regulation achieved with Cascode Current Mirror architecture is 4.932mV/V, while 5.77mV/V for Op –Amp Based architecture for an input variation of 2.6V to 3.6 V. The circuit has the PSRR of 80dB for Cascode Current Mirror architecture and 42.5dB for Op – Amp based BGR up to 110 Hz and 10 KHz respectively. The schematic entry and layouts of circuits were drawn using Cadence virtuoso 6.1.5 tool and assura verification tool was used for all verifications.

- The project entitled **IoT Based Real time System to Monitor Quality of Milk** carried out by Karthik Dhulashetty, Praveen N, Prerana R S and Pooja A R, under the guidance of Dr. G S Sunitha Prof. & Head was selected as **Best Project.**

  Abstract: The milk is the dietary fluid secreted by mammary glands of mammals. The high-quality milk should have better density and should be free from the adulterants. Milk is most commercially sold commodity both by local vendors as well as supermarkets. However, in local areas, to increase the yield certain adulterants are added which may affect the nutritional quality of milk. Consumption of adulterated milk causes serious health problems and is of great concern to the food industry. So, it is necessary to ensure the quality of milk by measuring the vital parameters present in the milk and the adulterants that are added to the milk. Here we are measuring the different parameters of milk such as pH, odor, temperature using sensors. Also, with the help of IOT process the milk vendors should be able to send the real time reading information of milk to the industries so that it helps to maintain the transparency.

LITERARY CONTRIBUTION

ಹೊರಡುಗುರಿಯೆಡೆಗೆ,ಹೋರಾಡು
ಜೀವನದೆಡೆಗೆಮುಟ್ಟುರಾರುನಿನ್ನನು,
ನಿನ್ನಗಟ್ಟಿತನವನು...
ಬಿಡು, ಭಯಅಂಜಿಕೆಯನೆರಳನು
ಸಾಧಿಸುವಫಲವಿರಲಿನಿನ್ನದೇಹಾದಿಯಲಿ
ನಿನಗೆನೀನೆಸಾಟಿನಿನಗೆನೀನೆಶಕ್ತಿ
ಕಾಣಲಿಯಶೋಗಾಥೆಸಿಂಹಾವಲೋಕನದಲಿ...
ನಿನ್ನಚರಿತ್ರೆಯಪುಟದಲಿ....

ಸುಚರಿತ S D
ಸಹಾಯಕಪ್ರಾಧ್ಯಾಪಕಿ
E & CE ವಿಭಾಗ

PAINTINGS

Spoorthi G N
4BD18EC104
VII ‘A’

Manjunath G M
4BD19EC055
V ‘B’

MOBILEPHOTOGRAPHY

Jhansi P M
4BD18EC046
VII ‘A’

Jhansi P M
4BD18EC046
VII ‘A’

Alumni Corner

Harsha Manjunath

Senior FAE in Tecnomic Components Pvt. Ltd.

About

Harsha Manjunath has a vast experience in FPGA Design and Verification. He is currently working as FAE in silicon Microsystems, Bangalore as VLSI front-end design and verification engineer. During his career Harsha Manjunath has been associated with organisations like HAL Bangalore, LRDE Bangalore, DARE Bangalore, BEL-CRL Bangalore, Bharat Dynamics Limited Hyderabad, Aeronautical Development Establishment (ADE)- Bangalore.

Experience

- Currently associated as a Senior FAE in Tecnomic Components PVT Ltd.
- Worked as FAE in Silicon Microsystems-Bangalore with 2.3-years of experience for VLSI front-end design and verification in FPGA, June 2004 to Oct 2006.
- Worked more than 10 years in FPGA Design and Verification.

Education

- **MS in VLSI-CAD from Manipal University Mangalore, 2012**
- **Bachelor of Engineering: Electronics and Communications, 1998 – 2002, BIET, Vishveswariah Technological University Belgaum**
- **STJ PU College, Davanagere 1996 - 1998**